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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/552,085	02/24/2000	Tsutomu Ishikawa		6265

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EXAMINER
NGUYEN, LONG T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/552,085	Applicant(s) ISHIKAWA ET AL.
	Examiner Long Nguyen	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed on 2/1/02 has been received and entered in the case.

2. The amendment filed on 2/1/02 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "the first value being higher than the second value" as discussed below in the 35 U.S.C. 112, 1st paragraph rejection.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The recitation "wherein an input impedance of an input stage circuit is set to a first value, and the parasitic capacitance is set to a second value, the first value being higher than the second value" is new matter because "the first value being higher than the second value" is not disclosed in the original specification.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 15, the recitation "wherein an input impedance of an input stage circuit is set to a first value, and the parasitic capacitance is set to a second value, the first value being higher than the second value" is indefinite because no comparison can be made between two things that have two different units. The "parasitic capacitance" has a unit of "farads" while the "input impedance" of a circuit is a complex number which is a combination of resistance, capacitance and inductance. Therefore, the "input impedance" and the "parasitic capacitance" do not have a one-to-one corresponding to each other.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 10-14 and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Bowers (USP 4,675,561).

With respect to claim 10, Figures 6-7 of the Bowers reference disclose a circuit a semiconductor integrated circuit which includes: a pad (62) to which an input signal (Vin) is externally inputted; a source follower circuit (FET2, I2) including a transistor (FET2) having a gate connected to the pad (62) and a source for producing an output signal (72); and it is inherent that a parasitic capacitance (of FET1) is created between said pad and a semiconductor substrate

(e.g. the parasitic capacitance between the gate and the body of FET1), and said source of the source follower circuit (e.g. source of FET2) is connected to the semiconductor substrate side of the parasitic capacitance (e.g. source of FET2 is connected to the body of FET1) "so as to charge and discharge the parasitic capacitance" (merely intended use) by the output signal of the source follower circuit (72).

With respect to claim 11, it is seen in Figure 7 of the Bowers reference that the semiconductor integrated circuit including an island region (74) on the upper surface of the semiconductor substrate (76) containing impurities of a second conductivity type (P), and a pad (82 or 88) formed on the island region via an oxide film; and wherein the semiconductor substrate contains impurities of a first conductivity type (N); and wherein an output terminal of the source follower circuit is connected to the island region.

With respect to claim 12, it is seen in Figure 7 that the island region (74) is surrounded with an isolation region (76) containing impurities of the first conductivity type (N).

With respect to claim 13, it is seen in the Bowers reference that the first conductivity type is a P-type and the second conductivity type is an N-type (Figure 7 and Col. 5, lines 42-48).

With respect to claim 14, it is seen in Figures 6-7 of the Bowers reference that the output terminal (source of FET2) of the source follower circuit is connected to the island region by way of a metal conductor.

With respect to claim 16, it is seen in Figure 6 that the input stage circuit includes an amplifier (FET2).

With respect to claim 17, it is seen in Figure 6 that the input stage circuit includes an FET transistor (FET2) integrated on the semiconductor substrate, the FET transistor having a gate connected to the pad.

With respect to claim 18, it is seen in Figure 6 that the FET transistor (FET2) has a drain connected to a power source, and a source connected to the ground via a constant current source (I2) for providing the output signal.

Response to Arguments

9. Applicant's arguments filed on 2/1/02 have been fully considered but they are not persuasive.

Applicant argues that the Bowers fails to teaches or suggests that "a parasitic capacitance is created between said pad and a semiconductor substrate, and said source of the source follower circuit is connected to the semiconductor substrate side of the parasitic capacitance so as to charge and discharge the parasitic capacitance by the output signal of said source follower circuit". However, the "parasitic capacitance" is seen to be inherent (e.g. the parasitic capacitance between the gate and the body of FET1 in Figure 6 of Bowers) because every MOSFET has parasitic capacitances between the body and the gate of the MOSFET (see Weste et al., Figure 4.5, page 184). Also, it is clearly in Figure 6 of the Bowers that the output (72) of the source follower circuit (FET2, I2) is connected to the body (substrate) of FET2 so it implies that the output (72) of the source follower circuit is connected to the substrate side of the parasitic capacitance. Furthermore, the recitation "so as so as to charge and discharge the parasitic capacitance by the output signal of said source follower circuit" is merely intended use and because the output (72) in Figure 6 is connected to the body of FET2 so it implies that the

output (72) of the source follower circuit charges and discharges that parasitic capacitance of FET2. Thus, for broad reasonable interpretation, all of the limitations in claim 10 are met because the structure of the claim is fully met by Bowers.

Conclusion

10. Because the scope of claim 15 cannot be determined, no prior can be applied against this claim.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Long Nguyen whose telephone number is (703) 308-6063. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 308-7722.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

May 10, 2002

LN

Long Nguyen
Art Unit: 2816

Terry D. Cunningham
Primary Examiner